REMARKS

Applicants acknowledge the indication that claims 8-11 contain allowable subject matter. Claims 1-16 are pending. Claims 4, 8, and 12-14 have been amended. No new matter has been added by way of this amendment. Reconsideration of the application is requested.

The drawings have been objected to under 37 C.F.R. 1.83(a). According to the Examiner, "the recitation 'transmission lines' in claim 6 must be shown or the feature(s) canceled from the claim(s)." In response to this objection, the following is noted. Each figure of the drawings clearly show lines that interconnect each of the specific circuit components. It is these lines that constitute the "transmission" lines set forth in the claims. Accordingly, Applicants respectfully assert that an amendment to the drawings is not necessary because the drawings clearly show this feature. Therefore, reconsideration and withdrawal of the objection to the drawings is respectfully requested.

The specification has been objected to by the Examiner. According to the Examiner, "'T11', 'T12', 'R3', and 'R4' as mentioned on line 14 at page 4 of the present specification are not shown on Figure 3A." In response to this objection, Applicants have amended the specification in a manner that is believed to resolve the discrepancy. Accordingly, reconsideration and withdrawal of the objection to the specification are respectfully requested.

Claims 4 and 13 have been objected to by the Examiner. As set forth in the Office Action, "'transmitters' on line 2 should be corrected as --transistors—and claim 13 is a duplicate of claim 12."

With respect to the objection to claim 4, Applicants have amended this claim along the lines as suggested by the Examiner. Accordingly, reconsideration and withdrawal of the objection are respectfully requested.

Regarding claim 13, it is true that this claim is a duplicate of claim 12. However, claim 12 depends from claim 7, while claim 13 depends from intermediate dependent claim 8 which depends from claim 7. Therefore, the combination of claims 7, 8, and 13 is not duplicative of the combination of claims 7 and 12. Accordingly, Applicants respectfully assert that claim 13 adds further limitations to claim 8, and is proper. Therefore, reconsideration and withdrawal of the objections to claim 13 are respectfully requested.

Claims 6-16 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

According to the Examiner, "it is unclear in claim 6 how the recitation 'transmission lines' is read on the preferred embodiment." With respect to this rejection, Applicants respectfully assert that "transmission lines" refers to the "wirings" used to interconnect specific circuit components, as noted by the Examiner. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

According to the Examiner, "it is unclear how the recitation 'at least one latch pair including two independent combined trans-admittance and trans-impedance stages' is read on the preferred embodiment. Insofar as understood, no such pair and stages can be determined on the drawings. Also, the recitation 'output current' on line 3 and 'stages' on line 4 is confusing because it is unclear if this is an additional 'output current' and 'stages' or a further recitation previously claimed 'output current' and 'stages' in claim 7." According to the Examiner, "the same is true for claims 9 and 15."

In response to the foregoing rejections, Applicants have amended the claims in a manner which is believed to resolve each specific rejection. Insofar as the rejection based on the interpretation of the drawings, Applicants draw the Examiner's attention to Fig. 2c and page 4, lines 3-9 of the specification. Set forth therein, is the statement that:

> "A chain may be formed by cascading a series of RL - TAS latches clocked on opposite phases of the system clock. Figure 2c is an exemplary symbol diagram of a cascaded latch chain in accordance with the present invention. The first TAS latch in the chain receives an input voltage Vin, Vinb and produces a current output Iout, Ioutb. By way of example, the chain in Figure 2c has two RL - TAS latches, however, any number of one or more RL - TAS latches may be cascaded together, as desired. Each RL - TAS latch receives a current Iin1, Iin1b and produces a current output Iout1, Iout1b." (Emphasis Added)

Applicants respectfully assert that this text when read in combination with Fig. 2c clearly provides how the recitation 'at least one latch pair including two independent combined trans-admittance and trans-impedance stages' is read on the preferred embodiment, where the "pair" and "stages" can be determined in the drawings. Accordingly, reconsideration and withdrawal of the rejection to the claims is respectfully requested.

Claim 7 stands rejected under 35 U.S.C. 102(b) as being anticipated by Fig. 1 of Applicants' admitted prior art, while claims 1, and 3-7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fig. 1 of Applicants' admitted prior art in view of U.S. Patent No. 3,917,959 to *Swiatowiec* et al. Claims 1-7 and 12-16 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,023,363 to *Harada* et al. These several rejections are respectfully traversed.

Claim 7 includes the limitation "a clocked trans-admittance stage latch receiving an input voltage and producing an output current."

Set forth on page 4 of the Office Action is the statement that:

> "The admitted prior art discloses in Figure 1 a latch circuit aa clocked trans-admittance stage latch (110 having transistors (T1-T6)) for receiving an input voltage (V_in) and producing an output current to the load resistors (R1, R2)."

With respect to the foregoing, Applicants respectfully assert that the admitted prior art fails to disclose that a clock trans-admittance stage latch receives an input voltage and produces an output current. In the circuit shown in Fig. 1, R1 and R2 are resistors that are respectively connected to the base of transistor T7 and T8, i.e., R1 and R2 are biasing resistors. A voltage supply V_{cc} is connected to one end of each resistor. This is straightforward circuit convention that indicates that the transistors are connected to a supply voltage V_{cc}. Moreover, the circuit clearly indicates that the outputs are voltages, i.e., V_outb and V_out. In fact, at each output of the circuit only output voltages are shown. In contrast, the invention set forth in claim 7 require an input voltage and an output current. Applicants respectfully assert that the prior art circuit shown in Fig. 1 is not configured, nor does it operate, in the manner as set forth in independent claim 7.

Therefore, reconsideration and withdrawal of the rejection under 35 U.S.C. §102(b) is respectfully requested.

U.S. Patent No. 3,917,959 to *Swiatowiec* et al. relates to a high speed counter circuit having set and reset capability that is also capable of operating in the gigahertz range (see col. 1, lines 15-17). According to this patent, an emitter-coupled logic latch is provided having active cascade load means for minimizing internal node capacitance and predetermined switchable active cascade load means for selectively setting and resetting latch stages for achieving gigahertz mode operation (see col. 1, lines 26-32). However, this reference fails to cure the deficiency of the described prior art of Applicants' invention as previously described.

Set forth on page 5 of the Office Action is the statement that:

> "The admitted prior art discloses in Figure 1 circuit comprising a clock trans-admittance circuit (110) having a first to second transistors (T1-T2) for receiving the signals (clk, clb), a third and fourth transistor for receiving the voltages (V-in, V_inb), and a load (120) but does not disclose that the load is the active load. Swiatowiec et al teaches in Figure 2 a latch circuit comprising an active load comprising transistors (122, 130) for adjusting the load resistance since the transistors (122, 130) function as the variable resistors. It would have been obvious to a person having skill in the art at the time the invention was made to employ the active load taught by Swiatowiec et al in the circuit of the admitted prior art for the purpose of adjusting the load resistance."

With respect to the foregoing, however, Applicants respectfully assert that the combination of the *Swiatowiec* et al. and the prior art described in Applicants' invention fails to disclose the invention as presently claimed. Specifically, the claimed invention as set forth in independent claims 1, 7, and 14 requires a clocked trans-admittance stage to receive an input voltage and to produce an output current. No where in the combination of the prior art described in Applicants' Fig. 1 and the *Swiatowiec* et al. reference is such a teaching found. Accordingly,

Applicants respectfully assert that independent claims 1, 7, and 14 are patentable over the combination of the cited references. Therefore, reconsideration and withdrawal of the rejection are respectfully requested.

U.S. Patent No. 6,023,363 to *Harada* et al. is directed to a wideband optical receiving apparatus or an optical receiving module for converting a digital optical signal into an electric signal and a technique particularly for improvement of frequency characteristics thereof (*see* col. 1, lines 5-9).

Set forth on page 4 of the Office Action is the statement that:

> "Harada et al discloses in Figure 6 a circuit comprising a two independent combined trans-admittance stage having transistors (T31-T34, T41, T42) and an active load having a trans-impedance stage (T11-T12). Note that the transmission lines are interpreted as the [wirings] used to connect the transistors together."

With respect to this rejection, the following is noted. Set forth in col. 7, line 64 thru col. 8, line 5 is the statement:

> "[T]he feedback amplification circuit of the present embodiment is what is called an AGC amplification circuit 105 (see FIG. 10), and is provided with a gain control circuit composed of two pairs of transistors T31, T32 and T33, T34 and what is called a transadmittance type amplification circuit including a pair of transistors T41 and T42. Among these circuits, collectors of the transistors T31, T33 and T32, T34 forming the gain control circuit are coupled in common with each other...."

With respect to the foregoing statement and with reference to Fig. 6, Applicants respectfully assert that each of the collectors of T31, T32, T33, and T34 are connected in common. In contrast, with reference to Fig. 2B of the present invention, in the area of the circuit that could possibly correspond to the area of the circuit selected by the Examiner in Fig. 6 of the *Harada* et al. patent,

namely transistors T5, T5', T6, and T6', none of the collectors are connected in common. Accordingly, the invention as set forth in independent claims 1, 7, and 14 differs in its fundamental configuration and operation from the circuit set forth in Fig. 6 of the *Harada* et al. patent.

In addition, according to the *Harada* et al. patent, "the non-inverted input signal InT and the inverted input signal InB...are current signals...these signals [are provided] to a circuit at a latter stage as a non-inverted output signal OutT or an inverted output signal OutB that are voltage signals." (see col. 8, lines 43-46).

In contrast, the present claimed invention requires an input voltage and an output current. The circuit of Fig. 6 shown in *Harada* et al. patent has this configuration reversed, i.e., the inputs are currents and the outputs are voltages. Accordingly, for this additional reason, Applicants respectfully assert that independent claims 1, 7, and 14 are not anticipated by the *Harada* et al. patent and therefore, reconsideration and withdrawal of the rejection are respectfully requested.

In view of the patentability of independent claims 1, 7, and 14 for the reasons set forth above, dependent claims 2-6, 8-13, and 15-16 are all patentable over the cited references.

Based on the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this Response, or the application in general, a telephone call to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

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Respectfully submitted,

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